

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : )

RAMKUMAR, et al. )

Serial No.: 09/635,507 )

Filed: August 9, 2000 )

For: PROCESS FOR REDUCING )  
LEAKAGE IN AN )  
INTEGRATED CIRCUIT )  
WITH SHALLOW TRENCH )  
ISOLATED ACTIVE AREAS )

RECEIVED

DEC 05 2003

TC 1700

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DEC 24 2003

TC 1700

DECLARATION TRAVERSING GROUNDS  
OF REJECTION UNDER 37 CFR § 1.132

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

I hereby declare:

1. I am making this DECLARATION in connection with a United States Patent Application entitled " PROCESS FOR REDUCING LEAKAGE IN AN INTEGRATED CIRCUIT WITH SHALLOW TRENCH ISOLATED ACTIVE AREAS" (hereinafter "the present patent application").

2. I am a Member of Technical Staff with ten (10) years of experience in the semiconductor processing industry.

3. I began working in the semiconductor industry in 1993 for Cypress Semiconductor.

4. I am currently employed at Cypress Semiconductor Corp.

5. I have used thermal processing and thin film deposition equipment for wafer fabrication for 10 years.

6. It is my understanding that currently available equipment used for High Density Plasma Chemical Vapor Deposition (HDPCVD) is not suitable for the thermal oxidation growth of an SiO<sub>2</sub> film on a silicon substrate, and is also not suitable for the subsequent annealing of the SiO<sub>2</sub> film.

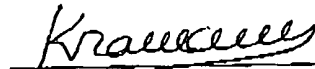
7. It is my understanding that currently available equipment used for High Density Plasma Chemical Vapor Deposition (HDPCVD) does not provide a heat source that may be used for the thermal oxidation growth of an SiO<sub>2</sub> film on a silicon substrate, and the subsequent annealing of the SiO<sub>2</sub> film.

12. I am one of the joint inventors of the invention disclosed in the present application.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code, and that such willful

false statements may jeopardize the validity of the present patent application or any patent issued thereon.

Dated: 24<sup>th</sup> November 2003



Krishnaswamy Ramkumar